What is claimed is:

1. A semiconductor memory device having a bank for storing a data and a port as a data I/O terminal, comprising:

a transmitter for delivering the data inputted from the port;

a global data bus for flowing an appearing current corresponding to the data outputted from the transmitter; and

a receiver for sensing the appearing current by using a current-mirror and delivering the data corresponding to the sensed appearing current into the bank,

wherein a swing range of a data bus voltage in response to the appearing current is narrower than a gap between a supply voltage and a ground.

2. The semiconductor memory device as recited in claim 1, wherein the supply voltage is supplied to the current mirror.

3. The semiconductor memory device as recited in claim 2, wherein the receiver includes:

a current mirror block for mirroring the appearing current of the global data bus to output a mirrored voltage as the data; and

a latch block for inverting the mirrored voltage outputted from the current mirror block and latching the converse mirrored voltage as the data to output the data into the port.

4. The semiconductor memory device as recited in claim 3, wherein the latch block includes:

an inverting block controlled by a data enable signal for inverting the mirrored voltage outputted from the current mirror block; and

a latch having two loop-connected inverters for latching the inverse mirrored voltage as the data to output the data into the port.

5. The semiconductor memory device as recited in claim 3, wherein the current mirror block includes:

a current mirror for mirroring the appearing current of the global data bus;

a current control block coupled between the current mirror and the global data bus for controlling amount of the appearing current; and

a switching block coupled to the current control block for enabling the output of the current mirror in response to a data control signal.

6. The semiconductor memory device as recited in claim 5, wherein the current mirror includes:

a first PMOS transistor having a gate, a drain and a source, the gate and drain diode-connected, the source connected to a supply voltage; and

a second PMOS transistor having a gate, a drain and a source, the drain connected to an output node, the source

connected to a supply voltage, the gate connected to the gate of the first PMOS transistor.

7. The semiconductor memory device as recited in claim 6, wherein the current control block includes:

a first NMOS transistor having a gate, a drain and a source, the gate coupled to a reference voltage, the source connected to the drain of the first PMOS transistor and the drain connected to the global data bus; and

a second NMOS transistor having a gate, a drain and a source, the gate coupled to the reference voltage, the source connected to the drain of the second PMOS transistor.

8. The semiconductor memory device as recited in claim 7, wherein the switching block includes

a third NMOS transistor having a gate, a drain and a source, the gate coupled to a data enable signal, the source connected to the drain of the second NMOS transistor and the drain connected to a ground.

9. The semiconductor memory device as recited in claim 4, wherein the inverting block includes:

a first PMOS transistor having a gate, a drain and a source, the gate coupled to the inverse data enable signal, the source connected to the supply voltage;

a second PMOS transistor having a gate, a drain and a source, the gate coupled to the first or second data outputted

from the mirroring block, the source connected to the drain of the first PMOS transistor, the drain coupled to the latch;

a first NMOS transistor having a gate, a drain and a source, the gate coupled to the data enable signal, the drain connected to a ground; and

a second NMOS transistor having a gate, a drain and a source, the gate coupled to the first or second data outputted from the mirroring block, the drain connected to the source of the first NMOS transistor, the source coupled to the latch.

10. The semiconductor memory device as recited in claim 1, wherein the transmitter includes

a NMOS transistor, coupled between the global data bus and a ground, having a gate coupled to the data.